AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended): A gate structure ~~with improved endurance characteristics~~, comprising:

~~a semiconductor region within~~ a substrate with source and drain regions;

~~source and drain regions contained within said semiconductor region;~~ at least a gate stack, disposed over said ~~semiconductor region~~ substrate, situated between said source and drain regions and containing a gate insulator layer ~~formed~~ over said ~~semiconductor region~~ substrate, a conductive gate layer disposed over said gate insulator layer, with nitrogen atoms incorporated along the conductive gate layer sidewall and the gate insulator layer-substrate interface.

2. (Original): The structure of claim 1 wherein a top gate stack layer is disposed over said conductive gate layer and a sidewall insulator layer, which could be an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride, is disposed over sidewalls of said gate stack.

3. (Cancelled).

4. (Currently amended): The structure of Claim 1 wherein said substrate ~~is a~~ comprises silicon ~~substrate~~.

5. (Original): The structure of Claim 1 wherein said gate insulator layer is an oxide layer.

6. (Original): The structure of Claim 1 wherein said conductive gate layer is a polysilicon layer.

7. (Original): The structure of Claim 1 wherein said conductive gate layer is a gate of a semiconductor integrated circuit device.

8. (Currently amended): The structure of Claim ~~1~~8 wherein said top gate stack layer is an insulator layer.

9. (Original): The structure of Claim 1 wherein said nitrogen atoms extend to the conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge.

10. (Currently amended): A gate structure for flash memory cells ~~with improved endurance characteristics~~, comprising:

~~a semiconductor region within~~ a substrate with source and drain regions;

~~source and drain regions contained within said semiconductor region;~~

at least a gate stack, disposed over said ~~semiconductor region~~ substrate, situated between said source and drain regions and containing a gate insulator layer ~~formed~~ over said ~~semiconductor region~~ substrate, a conductive floating gate layer over said gate insulator layer, an interpoly insulator layer disposed over said conductive gate layer, a conductive control gate layer and a top insulator layer and with a sidewall insulator layer disposed over sidewalls of said gate stack and with nitrogen atoms incorporated along the conductive gate layer sidewall-sidewall insulator layer interface and along the conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge and the gate insulator layer-substrate interface.

11. (Cancelled).

12. (Currently amended): The structure of Claim 10 wherein said substrate ~~is a~~ comprises silicon ~~substrate~~.

13. (Original): The structure of Claim 10 wherein said gate insulator layer is an oxide layer.

14. (Original): The structure of Claim 10 wherein said conductive floating gate layer is a polysilicon layer.

15. (Original): The structure of Claim 10 wherein said floating conductive gate layer is a floating gate of a stacked gate or of a split gate flash memory cell.

16. (Original): The structure of Claim 10 wherein said interpoly insulator layer is an ONO layer.

17. (Original): The structure of Claim 10 wherein said sidewall insulator layer is an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride.

18. (Original): The structure of Claim 10 wherein said conductive control gate layer is a polysilicon layer.

19. (Original): The structure of Claim 10 wherein said top insulator layer is an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride.

20. (Original): The structure of Claim 10 wherein a transfer gate stack, comprising:

said gate insulator layer;

a conductive transfer gate layer, that could be a polysilicon layer, disposed over said gate insulator layer;

a top transfer gate insulator layer, that could be an oxide layer or a nitride layer or a combination of these layers, disposed over said transfer gate layer ; and

a transfer gate sidewall insulator layer, that could be an oxide layer or a nitride layer or a combination of these layers; is situated between said gate stack and said source region.

21. (Currently amended): A method to fabricate a gate structure ~~with improved endurance characteristics~~, comprising:

providing ~~Providing a semiconductor region within~~ a substrate with source and drain regions;

~~Forming source and drain regions contained within said semiconductor region;~~

forming ~~Forming~~ at least a gate stack, disposed over said ~~semiconductor region~~ substrate, situated between said source and drain regions and containing a gate insulator layer ~~formed~~ over said ~~semiconductor region~~ substrate, a conductive gate layer disposed over said gate insulator layer and providing a nitrogen-based treatment on the sidewall of said conductive gate layer and the gate insulator layer-substrate interface.

22. (Cancelled).

23. (Currently amended): The method of Claim 21 wherein said substrate ~~is a~~ comprises silicon ~~substrate~~.

24. (Original): The method of Claim 21 wherein said gate insulator layer is an oxide layer.

25. (Original): The method of Claim 21 wherein said conductive gate layer is a polysilicon layer.

26. (Original): The method of Claim 21 wherein said conductive gate layer is a gate of a semiconductor integrated circuit device.

27. (Original): The method of Claim 21 wherein a top gate stack layer, which could be an insulator layer, is formed over said conductive gate layer.

28. (Original): The method of Claim 21 wherein a sidewall insulator layer, which could be an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride, is formed over sidewalls of said gate stack.

29. (Original): The method of Claim 21 wherein said nitrogen-based treatment is either a furnace anneal with NH_3 at a temperature of about 800 degrees Celsius for about 120 minutes or a RTA with NH3 at a temperature of about 1000 degrees Celsius for about 10 seconds.

30. (Currently amended): A method to fabricate a gate structure for flash memory cells ~~with improved endurance characteristics~~, comprising:

forming ~~a semiconductor region within~~ a substrate with source and drain regions;

~~forming source and drain regions contained within said semiconductor region;~~

forming at least a gate stack, disposed over said ~~semiconductor region~~ substrate, situated between said source and drain regions and containing a gate insulator layer ~~formed~~ over said ~~semiconductor region~~ substrate, a conductive floating gate layer disposed over said gate insulator layer, an interpoly insulator layer disposed over said conductive gate layer, a conductive control gate layer and a top insulator layer and with a sidewall insulator layer disposed over sidewalls of said gate stack and with a nitrogen treatment performed which further incorporated into the gate insulator layer-substrate interface before forming said sidewall insulator.

31. (Cancelled).

32. (Currently amended): The method of Claim 30 wherein said substrate ~~is a~~ comprises silicon ~~substrate~~.

33. (Original): The method of Claim 30 wherein said gate insulator layer is an oxide layer.

34. (Original): The method of Claim 30 wherein said conductive floating gate layer is a polysilicon layer.

35. (Original): The method of Claim 30 wherein said conductive floating gate layer is a floating gate of a split gate or of a stacked gate flash memory cell.

36. (Original): The method of Claim 30 wherein said interpoly insulator layer is an ONO layer.

37. (Original): The method of Claim 30 wherein said sidewall insulator layer is an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride.

38. (Original): The method of Claim 30 wherein said nitrogen treatment is either a furnace anneal with NH3 at a temperature of about 800 degrees Celsius for about 120 minutes or a RTA with NH3 at a temperature of about 1000 degrees Celsius for about 10 seconds.

39. (Original): The method of Claim 30 wherein said conductive control gate layer is a polysilicon layer.

40. (Original): The method of Claim 30 wherein said top insulator layer is an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride.

41. (Original): The method of Claim 30 wherein a transfer gate stack, comprising:

said gate insulator layer;

a conductive transfer gate layer, that could be a polysilicon layer, disposed over said gate insulator layer;

a top transfer gate insulator layer, that could be an oxide layer or a nitride layer or a combination of these layers, disposed over said transfer gate layer and a transfer gate sidewall insulator layer, that could be an oxide layer or a nitride layer or a combination of these layers; is situated between said gate stack and said source region.